AMENDMENTS TO THE CLAIMS

Claims 1-7 (Cancelled)

8. (Previously Presented) A method of forming a copper wiring in a semiconductor devices, the method comprising:

forming damascene patterns in an interlayer insulating film which is formed on a substrate;

sequentially forming a copper barrier metal layer and a copper seed layer on the surface of the interlayer insulating film including the damascene patterns;

performing a copper electroplating process in an electroplating apparatus to fill the damascene patterns with a copper layer by applying a negative (-) power supply to the substrate;

polishing the copper layer and the copper seed layer by means of a copper electro-polishing process in the electroplating apparatus by turning off the negative (-) power supply and applying a positive (+) power supply to the copper layer and the copper barrier layer until the copper barrier metal layer is exposed, thereby forming copper wirings within the damascene patterns; and

polishing the copper barrier metal layer by means of a chemical mechanical polishing process until the surface of the interlayer insulating film is exposed.

9. (Original) The method as claimed in claim 8, wherein the copper barrier metal layer is formed using one of ionized PVD TiN, CVD TiN, MOCVD TiN, ionized PVD Ta, ionized PVD TaN, CVD Ta, CVD TaN and CVD WN.

10. (Original) The method as claimed in claim 8, wherein the copper seed layer is formed using an ionized PVD method.

11. (Previously Presented) The method as claimed in claim 8, wherein the copper electroplating process comprises:

loading the substrate on which the copper seed layer is formed into the electroplating apparatus in which a copper plating solution including an organic accelerator and an organic suppressor are added;

setting a plating target range so that the damascene patterns could be sufficiently filled; and

applying the negative (-) power supply having current in the range of 1~5A to the substrate.

12. (Previously Presented) The method as claimed in claim 8, wherein the copper electroplating process comprises:

loading the substrate on which the copper seed layer is formed into the electroplating apparatus in which a copper plating solution including an organic accelerator, an organic suppressor and an organic leveler are added;

setting a plating target range so that the damascene patterns could be sufficiently filled; and

applying the negative (-) power supply having current in a range of 1~5A to the substrate.

13. (Previously Presented) The method as claimed in claim 8, wherein the copper electro-polishing process is performed by applying the positive (+) power supply having current in a range of 1~30A to the copper layer and the copper barrier metal layer, and stopping the electro-polishing if the copper barrier metal layer is exposed.

14. (Canceled)

15. (New) A method of forming a copper wiring in a semiconductor device, the method comprising:

forming damascene patterns in an interlayer insulating film which is formed on a substrate;

sequentially forming a copper barrier metal layer and a copper seed layer on the surface of the interlayer insulating film including the damascene patterns;

performing a copper electroplating process in an electroplating apparatus to fill the damascene patterns with a copper layer by applying a negative (-) power supply to the substrate;

changing a bias condition by turning off the negative (-) power supply and applying a positive (+) power supply to the copper layer and the copper barrier layer in the electroplating apparatus;

polishing the copper layer and the copper seed layer by means of a copper electro-polishing process in the electroplating apparatus until the copper barrier metal layer is exposed, thereby forming copper wirings within the damascene patterns; and

polishing the copper barrier metal layer by means of a chemical mechanical polishing process until the surface of the interlayer insulating film is exposed.

16. (New) The method as claimed in claim 15, wherein the copper barrier metal layer is formed using one of ionized PVD TiN, CVD TiN, MOCVD TiN, ionized PVD Ta, ionized PVD TaN, CVD Ta, CVD TaN and CVD WN.

17. (New) The method as claimed in claim 15, wherein the copper seed layer is formed using an ionized PVD method.

18. (New) The method as claimed in claim 15, wherein the copper electroplating process comprises:

loading the substrate on which the copper seed layer is formed into the electroplating apparatus in which a copper plating solution including an organic accelerator and an organic suppressor are added;

setting a plating target range so that the damascene patterns could be sufficiently filled; and

applying the negative (-) power supply having current in a range of 1~5A to the substrate.

19. (New) The method as claimed in claim 15, wherein the copper electroplating process comprises:

loading the substrate on which the copper seed layer is formed into the electroplating apparatus in which a copper plating solution including an organic accelerator, an organic suppressor and an organic leveler are added;

setting a plating target range so that the damascene patterns could be sufficiently filled; and

applying the negative (-) power supply having current in the range of 1~5A to the substrate.

20. (New) The method as claimed in claim 8, wherein changing the bias condition comprises applying a positive (+) power supply having current in a range of 1~30A to the copper layer and the copper barrier layer.